1. Shock & Drop / Vibration

Do not inflict excessive shock and mechanical vibration that exceeds the norm, such as hitting or mistakenly dropping, when transporting and mounting on a board. There are cases when pieces of crystal break, and pieces that are used become damaged, and become inoperable. When a shock or vibration that exceeds the norm has been inflicted, make sure to check the characteristics.

2. Cleaning

Since a crystal piece can be broken by resonance when a crystal device is cleaned by ultrasonic cleaning, be careful when carrying out ultrasonic cleaning.

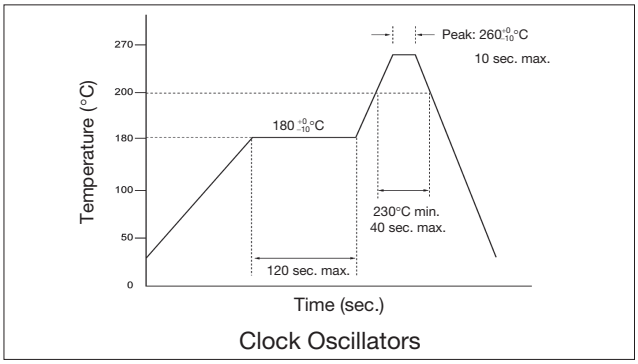
3. Soldering conditions

To maintain the product reliability, please follow recommended conditions.

Standard soldering iron conditions

	Clock Oscillators
Soldering iron	280°C to 340°C
Time	3+1/ −0 sec. max.

Reflow conditions (Example)



Recommended reflow Conditions vary depending upon products.
Please check with the respective specification for details.

4. Mounting Precautions

The lead of the device and the pattern of the board is soldered on the surface. Since extreme deformation of the board tears off the pattern, tears off the lead metal, cracks the solder and damages the sealed part of the device and there are cases in which performance deteriorates and operation fails, use it within the stipulated bending conditions. Due to the small cracks in the board resulting from mounting, please pay sufficient attention when attaching a device at the position where the warping of the board is great.
When using an automatic loading machine, as far as possible, select a type that has a small impact and use it while confirming that there is no damage.
Surface mount devices are NOT flow soldering compatible.

5. Storage Condition

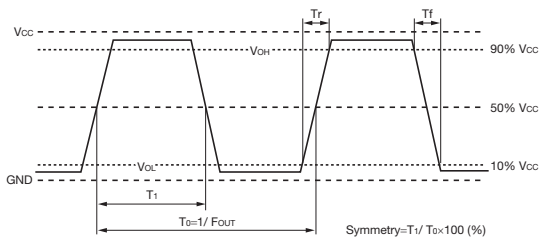
Since the long hour high temperature and low temperature storage, as well as the storage at high humidity are causes of deterioration in frequency accuracy and solderability.
Parts should be stored in temperature range of −5 to +40°C, humidity 40 to 60% RH, and avoid direct sunlight. Then use within 6 months.

6. In order to use clock oscillators

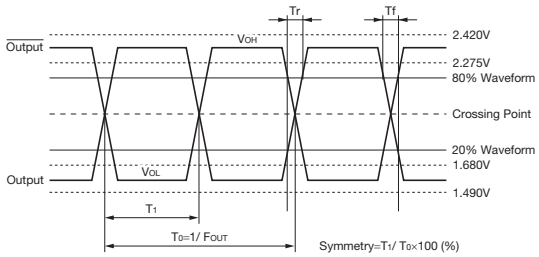
(1) The miniature oscillator for the clock utillzes a CMOS IC and incorporates a protective circuit against static electricity. However, exercise care in the same manner as for a normal CMOS IC.
(2) Internal capacitor is not provided in the power supply section (+DC-GND). *
To serve as overimpressed voltage and overcurrent protective device, place a bypass capacitor (0.01µF) as near as possible to the (+DC-GND) terminal. However, the capacitance value is meant as a guideline. Depending on the capacitor type, frequency characteristics vary. Accordingly, use a capacitor that matches the frequency characteristics.
* KC7050S series has Bypass Capacitior between Vcc and GND.
(3) Applying reverse voltage could result in damage to internal parts. Take care not to connect terminals incorrectly.
(4) Please do not use oscillators under unfavorable condition such as beyond specified range in catalog or specification sheet.
(5) Please keep oscillators away from water, salt water or harmful gas.
(6) KC7050S series should be stored in humidity-controlled area after the package is unsealed, in temperature +25±5°C, under humidity of 65%RH, and should be mounted on PCB within 7 days.
(7) Frequency drift may occur as a result of application of light such as direct sunlight or LED light etc when operating clock oscillator Z series MC-Z series.
Please use in a design and environment that consider light shielding.
Note the frequency drift will not occur if used in a light-shielded environment.

Clock Timing Chart

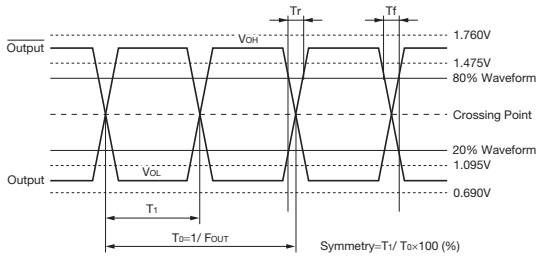
[CMOS Output]



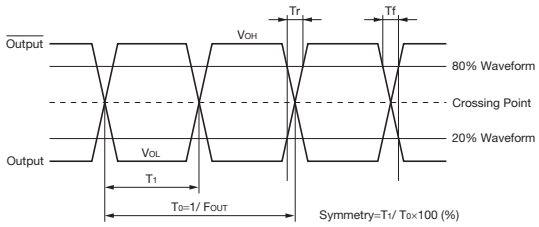
[LV-PECL (3.3V) Output]



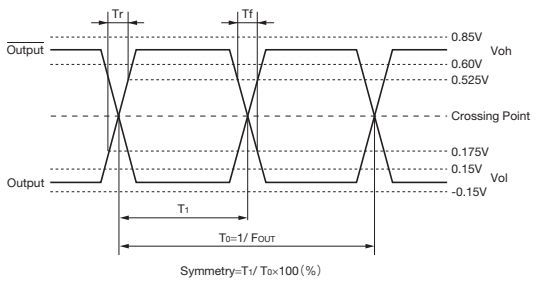
[LV-PECL (2.5V) Output]



[LVDS Output]

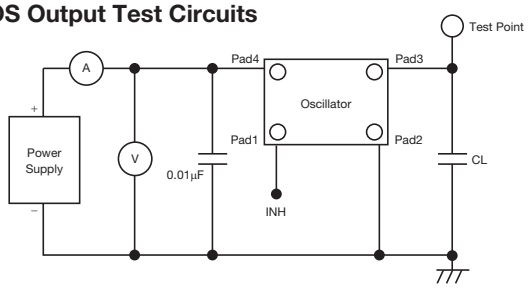


[HCSL-Output]



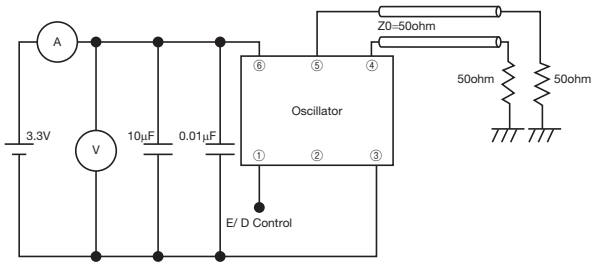
Test Circuits

CMOS Output Test Circuits

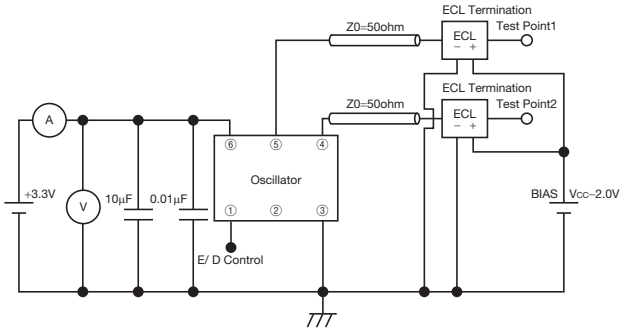


Note) Maximum load (Includes capacitances of fixture and probe)

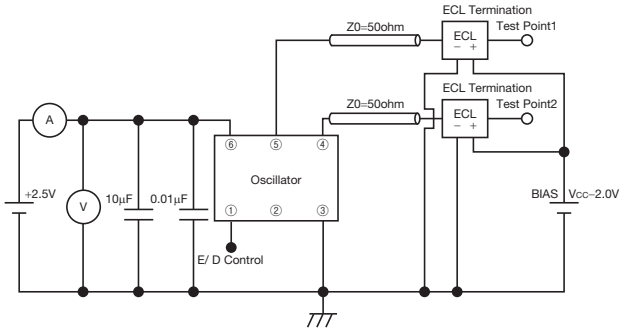
HCSL Output Test Circuits



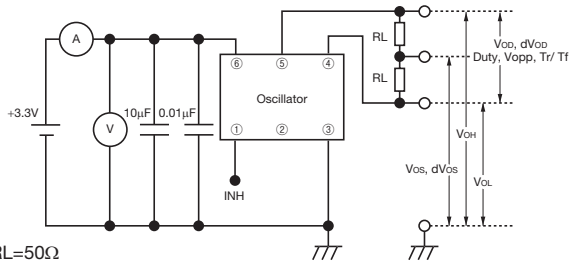
LV-PECL (3.3V/ XO) Output Test Circuits



LV-PECL (2.5V/ XO) Output Test Circuits

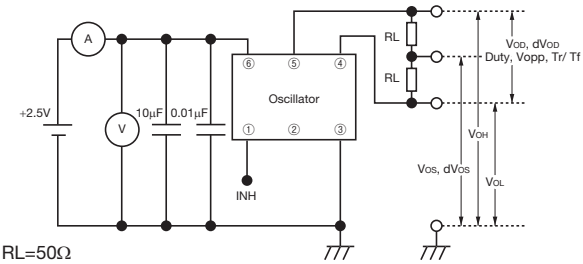


LVDS (3.3V/ XO) Output Test Circuits



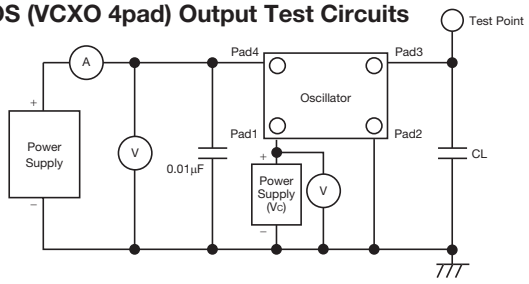
Note) RL=50Ω

LVDS (2.5V/ XO) Output Test Circuits



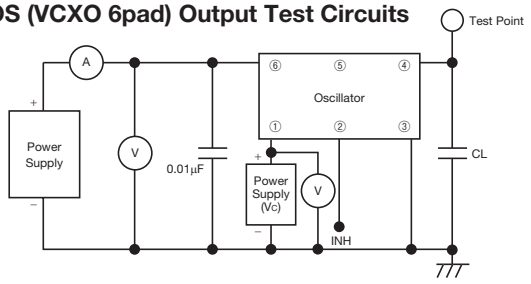
Note) RL=50Ω

CMOS (VCXO 4pad) Output Test Circuits



Note) Maximum load (Includes capacitances of fixture and probe)

CMOS (VCXO 6pad) Output Test Circuits



Note) Maximum load (Includes capacitances of fixture and probe)